UDC 004.052.32+681.518.5

V. V. Sapozhnikov, D. Eng. Sci.,
Vl. V. Sapozhnikov, D. Eng. Sci.

The Department of "Automation and Remote Control on Railways",
Emperor Alexander I St. Petersburg State Transport University,
Saint Petersburg, Russian Federation

D. V. Efanov, D. Eng. Sci.

"VEGA Group" LLC, Saint Petersburg, Russian Federation;
Higher School of Transport, Institute of Mechanical Engineering, Materials and Transport,
Peter the Great St. Petersburg Polytechnic University, Saint Petersburg, Russian Federation;
The Department of "Automation, Remote Control and Communication on Railway Transport",
Russian University of Transport, Moscow, Russian Federation

THE FEATURES OF THE COMBINATIONAL LOGIC CIRCUITS CONCURRENT ERROR-DETECTION SYSTEMS BASED ON THE SEARCH FOR SYMMETRICALLY-INDEPENDENT OUTPUTS GROUPS CONSTRUCTION

The authors of the article found that in the use of classical sum codes (Berger codes) and a some of their modifications in the combinational circuits testing organization it is possible to detect both unidirectional and part of non-unidirectional errors in the data vectors. It is shown that it is possible to search for such groups of outputs of combinational circuits where only symmetrical errors occur due to stuck at-faults of elements of the internal structure of the circuits. Such groups of outputs are designated as symmetrically-independent outputs (SI-groups of outputs). The conditions of belonging of the group of outputs of the combinational circuits to the SI-groups of outputs are determined. It is shown that each SI-group of outputs can be controlled using a separate testing subsystem based on the code with the detection of any non-symmetrical errors (in particular, and any non-symmetrical errors up to certain multiplicities). The ways of searching for SI-groups of outputs in the combinational circuits testing organization are presented.

Combinational circuit, self-checking structure, unidirectional error, symmetrical error, asymmetrical error, code with the unidirectional and asymmetrical error detection, groups of symmetrically-independent outputs

DOI: 10.20295/2412-9186-2020-6-4-532-549

1. Introduction

The methods of redundant coding are widely used in the self-checking discrete devices developing. These methods are used both at the stages of automata synthesis and at the organization of test and functional diagnosis systems [1, 2]. The features of error detection by redundant codes allow developers of discrete devices to give the properties of testability and fault detection to their structures [3].

The redundant coding is also used in the testing organization of the combinational components of discrete devices, or combination logic circuits [4]. The use of redundant coding in this case implies, on the one hand, taking into account the characteristics of error detection by the certain code, and on the other hand, taking into account the structural features of the combinational circuits themselves. Among such properties of codes, it is possible to allocate possibilities of certain type's error detection (combinations of ones and zero bits distortions) and multiplicities (number of the bits distorted at an error) [5]. From the standpoint of the combinational circuit structure it is the characteristics of its implementation: ranking of logic elements (or element groups) in the structure, the relationships between them, the presence of branches, the number of paths between the poles of the circuit with odd and even number of inversions, etc. [6]. In this situation, there are two possible ways. The first way consists in choosing a code "for" a given circuit structure: searching for a code with the desired features or selecting groups of circuit outputs for separate control by one or another attribute, etc. The second way involves a special transformation of the combinational circuit structure into some structure that is controllable by the selected code. It should be such a structure that allows occurrence of errors only of a certain type or multiplicities.

The codes that are focused on the detection and not on the correction of faults are most commonly used in the synthesis of fault detection combinational circuits. This makes it possible to obtain devices with a relatively small structural redundancy (as a rule, compared to duplication and subsequent comparison of the values of the self-titled outputs [7]). Among these codes are parity codes [8], constant-weight codes [9], codes with summation (Berger codes) [10] and their various modifications [11–13]. For example, parity codes do not detect any errors with even multiplicities, but they detect any single distortions. This property of parity codes is effectively used in organizing of the control of combinational circuits by groups of independent outputs (I-groups of outputs) or after converting the circuit structure into a circuit with one I-group of outputs [14–16]. Another example is the use of constant-weight codes and classical Berger codes with the property of detecting any unidirectional errors (this property of these codes is often used). In this case, either the search for groups of unidirectionally-independent outputs (UI-groups of outputs) is performed, or the transformation of the circuit structure into a circuit with one UI-group of outputs [17, 18]. It is possible to take into account other features of redundant codes and structures of controlled combinational circuits [19, 20].

This paper is devoted to the description of the key results of the research of the development of testing methods for combinational circuits based on the properties of codes aimed at detecting errors of certain types and multiplicities. It is proposed to organize testing of combinational circuits by the property of detecting any errors, except for multidirectional errors of even multiplicity, associated with the simultaneous distortion of the same number of zero and ones bits (symmetrical errors). This property is possessed by both constant-weight codes and Berger codes and some of their modifications.

2. Types of errors and codes with the detection of certain types of errors

The classification of errors in vectors of redundant codes proposed in [5] implies their division into several types: symmetrical, unidirectional, and asymmetrical errors. *Symmetrical* errors are associated with the simultaneous distortion of the same number of zero and ones bits. *Unidirectional* errors include errors caused by distortions of only zero or only ones bits. *Asymmetrical* errors occur while distorting an unequal number of zero and ones bits. It should be noted that these types of errors are distributed in various proportions in the code vectors depending on their lengths. With an increase in the length of the code vector, the proportion of asymmetrical errors increases, while the proportion of unidirectional errors gradually, while symmetrical errors, slightly decreases. For example, for the case $m = 10$, subject to the formation of a full set of output combinations, the proportion of unidirectional errors is approximately 0.2 %, symmetrical — 24.6 %, and asymmetrical — 75.2 %.

Among the variety of codes aimed at detecting errors, special classes of codes are detected that detect any unidirectional errors or any unidirectional errors up to the established multiplicity d_υ — the so-called $UED\,(m, k)$ and d_υ-$UED\,(m, k)$ codes. Such codes, for example, include Berger codes and Bose-Lin codes (modular sum codes). Berger codes are $UED\,(m, k)$-codes, and Bose-Lin codes are d_υ-$UED\,(m, k)$, where the d_υ value is determined by the value of the module selected when constructing the code [21, 22].

In [23], it was shown that in self-checking devices constructing, the possibility of detecting by some codes, in addition to any unidirectional errors, also any asymmetrical errors in data vectors can also be taken into account. We introduce the class of codes with the detection of any unidirectional and asymmetrical errors — $UAED\,(m, k)$-codes, as well as the class of codes with the detection of any unidirectional and asymmetrical errors to the established values of the multiplicities d_υ and d_α, respectively — d_υ, d_α-$UAED\,(m, k)$-codes. Taking into account the features of $UAED\,(m, k)$ and d_υ, d_α-$UAED\,(m, k)$-codes allows us to reduce the structural redundancy of the synthesized discrete devices.

In organizing of combinational circuits control with using $UAED\,(m, k)$ and d_υ, d_α-$UAED\,(m, k)$-codes, the two approaches described above are also possible, however, the UI-groups expand to the so-called unidirectionally/asymmetrically-independent output groups (UAI-groups). This allows us to simplify the final structures of self-checking combinational circuits.

The search for UAI-groups of outputs is similar to the search for groups of outputs that allow only symmetrical distortions. Here we describe the search conditions for such output groups of combinational circuits.

3. Search terms for checkable output groups

We introduce the following notation: $\{f_1, f_2, ..., f_m\}$ is set of combinational circuit outputs; $\{x_1, x_2, ..., x_n\}$ is set of combinational circuit inputs; $\omega_t^{a_r} = \{f_{j_1}, f_{j_2}, ..., f_{j_q}\}$ is

a subset of combinational circuit outputs, ($j_1, j_2, ..., j_q \in \{1,2,...,m\}$), which are distorted when the output element failure with the value of the output function y_t (element G_t) is input into the device and when the binary vector $a_r = \langle x_1 x_2 ... x_n \rangle$, where a_r is a binary decimal equivalent, $a_r \in \{0,1,...,2^n\}$, $q \in \{2,3,...,m\}$ receipts on the input.

Consider the combinational circuits shown in Fig. 1.

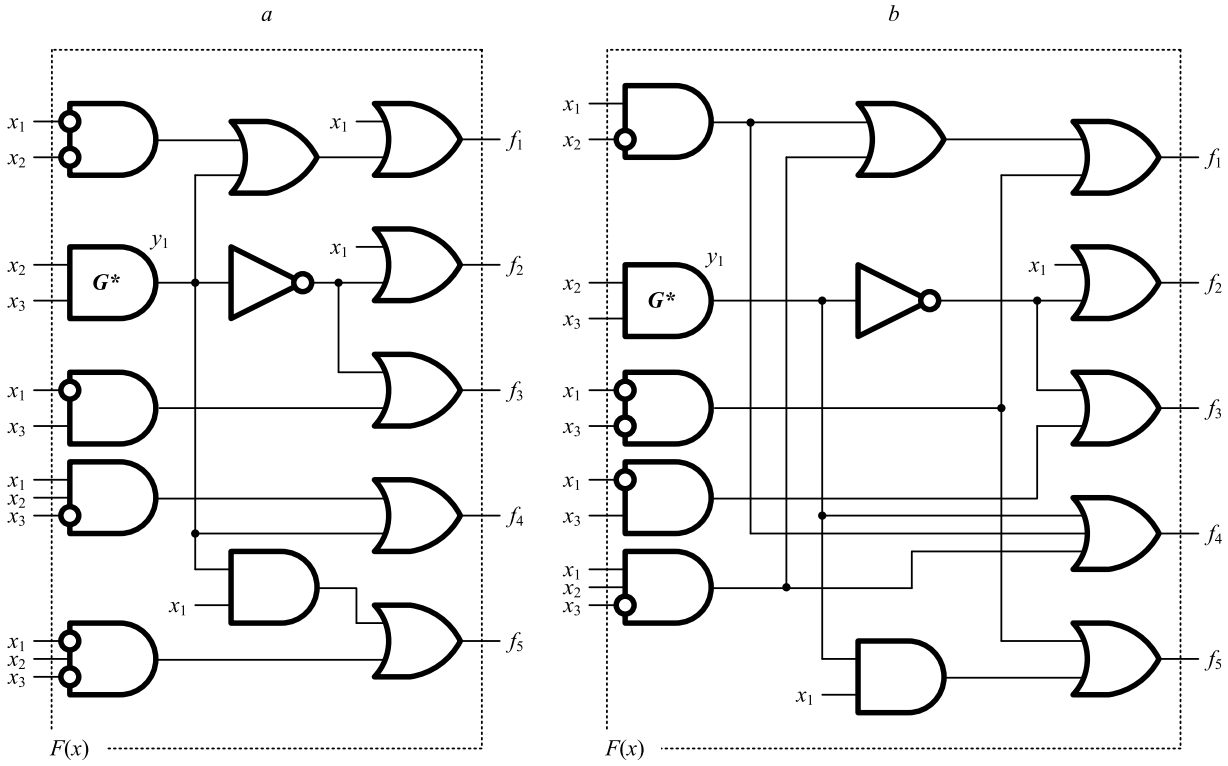

Figure 1. The combinational circuit in which a symmetrical error may occur at the outputs (*a*), and the combinational circuit in which a symmetrical error at the outputs are eliminated (*b*)

The circuit shown in Fig. 1, *a* refers to circuits at the outputs of which a symmetrical error may occur (Table 1). For this we have:

$$\omega_1^0 = \{f_2, f_3, f_4\};$$

$$\omega_1^1 = \{f_2, f_4\};$$

$$\omega_1^2 = \{f_1, f_2, f_3, f_4\};$$

$$\omega_1^3 = \{f_1, f_2, f_4\};$$

$$\omega_1^4 = \{f_3, f_4, f_5\};$$

$$\omega_1^5 = \{f_3, f_4, f_5\};$$

Table 1. The description of the operation of circuit Fig. 1, *a* in the event of faults in the logic element *G**

x_1	x_2	x_3	f_1	f_2	f_3	f_4	f_5	$\frac{\partial f_1}{\partial y_1}$	$\frac{\partial f_2}{\partial y_1}$	$\frac{\partial f_3}{\partial y_1}$	$\frac{\partial f_4}{\partial y_1}$	$\frac{\partial f_5}{\partial y_1}$
0	0	0	1	1	1	0	0	0	1 (1→0)	1 (1→0)	1 (0→1)	0
0	0	1	1	1	1	0	0	0	1 (1→0)	0	1 (0→1)	0
0	1	0	0	1	1	0	1	1 (0→1)	1 (1→0)	1 (1→0)	1 (0→1)	0
0	1	1	1	0	1	1	0	1 (1→0)	1 (0→1)	0	1 (1→0)	0
1	0	0	1	1	1	0	0	0	0	1 (1→0)	1 (0→1)	1 (0→1)
1	0	1	1	1	1	0	0	0	0	1 (1→0)	1 (0→1)	1 (0→1)
1	1	0	1	1	1	1	0	0	0	1 (1→0)	0	1 (0→1)
1	1	1	1	1	0	1	1	0	0	1 (0→1)	1 (1→0)	1 (1→0)

$$\omega_1^6 = \{f_3, f_5\};$$

$$\omega_1^7 = \{f_3, f_4, f_5\}.$$

At the outputs of the circuit depicted in Fig. 1, *b*, despite the topology, the occurrence of symmetrical errors is excluded (Table 2). For this we have:

$$\omega_1^0 = \{f_2, f_3, f_4\};$$

$$\omega_1^1 = \{f_1, f_2, f_4, f_5\};$$

$$\omega_1^2 = \{f_2, f_3, f_4\};$$

$$\omega_1^3 = \{f_1, f_2, f_4, f_5\};$$

$$\omega_1^4 = \{\varnothing\};$$

$$\omega_1^5 = \{\varnothing\};$$

$$\omega_1^6 = \{\varnothing\};$$

$$\omega_1^7 = \{f_1, f_3, f_4\}.$$

Table 2. The description of the operation of circuit Fig. 1, *b* in the event of faults in the logic element *G**

x_1	x_2	x_3	f_1	f_2	f_3	f_4	f_5	$\frac{\partial f_1}{\partial y_1}$	$\frac{\partial f_2}{\partial y_1}$	$\frac{\partial f_3}{\partial y_1}$	$\frac{\partial f_4}{\partial y_1}$	$\frac{\partial f_5}{\partial y_1}$
0	0	0	1	1	1	0	1	0	1 (1→0)	1 (1→0)	1 (0→1)	0
0	0	1	0	1	1	0	0	1 (0→1)	1 (1→0)	0	1 (0→1)	1 (0→1)
0	1	0	1	1	1	0	1	0	1 (1→0)	1 (1→0)	1 (0→1)	0
0	1	1	1	0	1	1	1	1 (1→0)	1 (0→1)	0	1 (1→0)	1 (1→0)
1	0	0	1	1	1	1	0	0	0	1 (1→0)	0	0
1	0	1	1	1	1	1	0	0	0	1 (1→0)	0	0
1	1	0	1	1	1	1	0	0	0	1 (1→0)	0	0
1	1	1	1	1	0	1	0	1 (1→0)	0	1 (0→1)	1 (1→0)	0

We denote by V_t the set of different subsets $\omega_t^{a_r}$ with an even number of elements; if there are several identical subsets $\omega_t^{a_r}$, any one of them is included in the set V_t.

For Fig. 1, *a* we have: $V_1 = \{\omega_1^2 = \{f_1, f_2, f_3, f_4\}, \omega_1^1 = \{f_2, f_4\}, \omega_1^6 = \{f_3, f_5\}\}$.

For Fig. 1, *b* we have: $V_1 = \{\omega_1^1 = \{f_1, f_2, f_4, f_5\}\}$.

A subset of the outputs of the combinational circuit $\{f_{j_1}, f_{j_2}, ..., f_{j_q}\}$ ($j_1, j_2, ..., j_q \in$ $\in \{1, 2, ..., m\}$) is called *a symmetrically-independent group* (*SI-group*) if the failure of the output of any element G_t in the device structure does not cause a symmetrical type error on these outputs.

Theorem 1. *A failure of the output of the element G_t does not cause a symmetrical type error on the set of outputs of the control unit $W = \{f_{j_1}, f_{j_2}, ..., f_{j_p}\}$, $p \in \{2, 3, ..., m\}$, if the following condition*:

$$\frac{\partial f_{k_1}}{\partial y_t} \cdot \frac{\partial f_{k_2}}{\partial y_t} \cdot ... \cdot \frac{\partial f_{k_d}}{\partial y_t} \cdot \left(\overline{\frac{\partial f_{h_1}}{\partial y_t}} \cdot \overline{\frac{\partial f_{h_2}}{\partial y_t}} \cdot ... \cdot \overline{\frac{\partial f_{h_{p-d}}}{\partial y_t}} \right) Q\left(R_d^{d/2}\left(f_{k_1}, f_{k_2}, ..., f_{k_d}\right)\right) = 0, \quad (1)$$

is satisfied for each subset $\omega_t^{a_r} = \{f_{k_1}, f_{k_2}, ..., f_{k_d}\}$, such that $\omega_t^{a_r} \in W$ и $\omega_t^{a_r} \in V_t$, where $f_{h_1}, f_{h_2}, ..., f_{h_{p-d}} \in \{f_{j_1}, f_{j_2}, ..., f_{j_p}\} \setminus \{f_{k_1}, f_{k_2}, ..., f_{k_d}\}$; the function $R_d^{d/2}(f_{k_1}, f_{k_2}, ..., f_{k_d})$ is a conjunction disjunction $f_{k_1} f_{k_2} \cdot ... \cdot f_{k_d}$, $f_k \in \{0,1\}$, in which the $\frac{d}{2}$ variables have direct values, and the rest of $\frac{d}{2}$ the variables have inverse values, and the function $Q\left(R_d^{d/2}\left(f_{k_1}, f_{k_2}, ..., f_{k_d}\right)\right)$ is a function obtained by substituting into a function $R_d^{d/2}$

instead of designating the output functions f_i their representations through input variables.

Proof. Consider the left side of the equality (1). We introduce the following notation:

$$A(y_t)=\frac{\partial f_{k_1}}{\partial y_t}\cdot\frac{\partial f_{k_2}}{\partial y_t}\cdot\ldots\cdot\frac{\partial f_{k_d}}{\partial y_t},\ B(y_t)=\frac{\overline{\partial f_{h_1}}}{\partial y_t}\cdot\frac{\overline{\partial f_{h_2}}}{\partial y_t}\cdot\ldots\cdot\frac{\overline{\partial f_{h_{p-d}}}}{\partial y_t},$$

$$C=Q\left(R_d^{d/2}\left(f_{k_1},f_{k_2},\ldots,f_{k_d}\right)\right).$$

In accordance with the this theorem, in studying the element G_t, it is necessary to consider all possible subsets of outputs $\omega_t^{a_r}$, that are distorted when one or more vectors of input variables are received at the device input. In this case, it is enough to consider only subsets with an even number of elements, because on subsets with an odd number of outputs it is impossible to generate errors of a symmetrical type. The second feature of the considered subsets $\omega_t^{a_r}$ is that when the input vector a_r arrives, the values of all the outputs included in the subset are distorted, and any other outputs are not distorted.

All subsets $\omega_t^{a_r}$ with the indicated properties are included by construction in the set V_t and must be considered by the hypothesis of the theorem. There are no other subsets $\omega_t^{a_r}$ other than those indicated above.

In accordance with the hypothesis of the theorem, each subset $\omega_t^{a_r}\in V_t$ is considered separately.

The left side of the equation (1) contains three cofactors: $A(y_t)$, $B(y_t)$ and C. The expression $A(y_t)$ defines those input vectors, upon receipt of which the values of all the outputs included in the considered subset $\omega_t^{a_r}$ are distorted. The expression $B(y_t)$ captures those input vectors, upon receipt of which all the outputs of the device that are not included in the subsets $\omega_t^{a_r}$ are not distorted. The product $A(y_t)B(y_t)$ allows you to calculate all those input vectors, upon receipt of which only those outputs that are part of a subset $\omega_t^{a_r}$ (and all at the same time) are distorted, and not one of the outputs that do not belong to this subset is distorted. It is necessary to check the possibility of a symmetrical error especially for these input vectors.

For this purpose, the left part of expression (1) includes the cofactor C, which allows calculating the $D\left(\omega_t^{a_r}\right)$ set of all input vectors, upon receipt of which, in principle, symmetrical errors may occur. A symmetrical error is possible if the half of the output functions on the input vector in a subset $\omega_t^{a_r}$ take the value 0, and the rest take the value 1. An expression $R_d^{d/2}\left(f_{k_1},f_{k_2},\ldots,f_{k_d}\right)$, represented as a function that depends on variables $f_{k_1},f_{k_2},\ldots,f_{k_d}$, defines combinations of these variables that meet the specified condition. The replacing in this expression the notation of the output functions by their representations through the input variables allows us to define the set $D\left(\omega_t^{a_r}\right)$.

If $A(y_t)B(y_t)C \neq 0$, then this means that there is at least one input vector, upon receipt of which a symmetrical error occurs. If there is an expression $A(y_t)B(y_t)C = 0$ for all subsets $\omega_t^{a_r} \in V_t$, then the failure of the output of the element G_t on the considered set W of the outputs of the combinational circuit does not cause symmetrical errors on any input vector.

The theorem is proved.

For the circuit of Fig. 1, *a* we consider the set $W = \{f_1, f_2, f_3, f_4, f_5\}$ and the element G^*. To verify the conditions of the theorem regarding the element G^* it is necessary to verify condition (1) for three subsets: $\{f_2, f_4\}$, $\{f_3, f_5\}$ and $\{f_1, f_2, f_3, f_4\}$.

For the subset $\{f_2, f_4\}$ we have:

$$\frac{\partial f_2}{\partial y_1} \cdot \frac{\partial f_4}{\partial y_1} \cdot \left(\overline{\frac{\partial f_1}{\partial y_1}} \cdot \overline{\frac{\partial f_3}{\partial y_1}} \cdot \overline{\frac{\partial f_5}{\partial y_1}} \right) \cdot Q\left(R_d^{d/2}(f_2, f_4) \right). \tag{2}$$

We calculate the derivatives (see formula (2) and Table 1):

$$\frac{\partial f_1}{\partial y_1} = \overline{x_1} x_2, \ \frac{\partial f_2}{\partial y_1} = \overline{x_1}, \ \frac{\partial f_3}{\partial y_1} = x_1 \vee \overline{x_1 x_3}, \ \frac{\partial f_4}{\partial y_1} = \overline{x_1} \vee x_1 \overline{x_2} \vee x_1 x_3, \ \frac{\partial f_5}{\partial y_1} = x_1.$$

We calculate the following expressions for checking the condition (1):

$$A(y_t) = \frac{\partial f_2}{\partial y_1} \cdot \frac{\partial f_4}{\partial y_1} = \overline{x_1} \left(\overline{x_1} \vee x_1 \overline{x_2} \vee x_1 x_3 \right) = \overline{x_1}; \tag{3}$$

$$B(y_t) = \overline{\frac{\partial f_1}{\partial y_1}} \cdot \overline{\frac{\partial f_3}{\partial y_1}} \cdot \overline{\frac{\partial f_5}{\partial y_1}} = \overline{\overline{x_1} x_2} \cdot \overline{x_1 \vee \overline{x_1 x_3}} \cdot \overline{x_1} = \overline{x_1 x_2} x_3; \tag{4}$$

$$R_d^{d/2}(f_2, f_4) = f_2 \overline{f_4} \vee \overline{f_2} f_4;$$

$$Q\left(R_d^{d/2}(f_2, f_4) \right) = \left(x_1 \vee \overline{x_1 x_2} \right) \overline{x_1 x_2 \vee x_2 x_3} \vee \overline{x_1 \vee \overline{x_1 x_2}} \left(x_1 x_2 \vee x_2 x_3 \right) = \overline{x_1} \vee x_1 \overline{x_2}. \tag{5}$$

As a result, we have:

$$\overline{x_1} \cdot \overline{x_1 x_2} x_3 \cdot \left(\overline{x_1} \vee x_1 \overline{x_2} \right) = \overline{x_1 x_2} x_3 \neq 0.$$

Since the left side of the obtained expression is not equal to zero, the condition of the theorem is not fulfilled and the fault of the element G^* causes a symmetrical error. The left side of the resulting expression defines a function that defines the input vectors for which this error occurs. In this case, it is a vector $\overline{x_1 x_2} x_3$.

For the circuit, shown in Fig. 1, *b*, we also consider the subset $\{f_1,f_2,f_3,f_4,f_5\}$ and the element *G**. In this case, verification of condition (1) is required for only one subset $\{f_1,f_2,f_4,f_5\}$.

In this case

$$R_d^{d/2}(f_1,f_2,f_4,f_5)=$$
$$=f_1f_2\overline{f_4}\,\overline{f_5}\vee f_1\overline{f_2}f_4\overline{f_5}\vee f_1\overline{f_2}\,\overline{f_4}f_5\vee\overline{f_1}f_2f_4\overline{f_5}\vee\overline{f_1}f_2\overline{f_4}f_5\vee\overline{f_1}\,\overline{f_2}f_4f_5,$$

$$Q\left(R_d^{d/2}(f_1,f_2,f_4,f_5)\right)=0.$$

Therefore, condition (1) is satisfied and the failure of the element *G** does not cause symmetrical errors on the set of all outputs of the circuit.

The following statement is obvious.

Theorem 2. *A subset of the outputs of the combinational circuit* $\{f_{j_1},f_{j_2},...,f_{j_p}\}$ $(j_1,j_2,...,j_p\in\{1,2,...,m\})$ *is a SI-group when each element in its structure satisfies the conditions of Theorem 1.*

Based on Theorems 1 and 2, it is possible to construct effective algorithms for searching for SI-groups of outputs and using these groups to obtain completely verifiable structures of combinational logic circuits using *UAED* (*m*, *k*) and d_υ, d_α-*UAED* (*m*, *k*) codes by analogy with how this was done in [3, 18].

4. The inputs of the logic elements fault detection

In all studies devoted to the synthesis and analysis of self-checking discrete devices, only stuck at-faults of the outputs of logic elements are considered and modeled. However, stuck at-faults also include faults in the individual inputs of the elements that are connected to the inputs of the device. For example, the previously considered circuit (Fig. 1, *a*) contains 13 stuck at-faults of the outputs of the logic elements and 15 stuck at-faults of the inputs of the logic elements.

Condition (1) allows us to formulate the following statement.

Theorem 3. *If a fault in the output of a logic element in a combinational circuit does not cause a symmetrical type error on the set of outputs of the device* $\{f_{j_1},f_{j_2},...,f_{j_p}\}$ $(j_1,\ j_2,...,j_p\in\{1,2,...,m\})$*, then a stuck at-faults in the input of the same element does not cause the same error.*

Proof. In fact, consider the element *G* at the output of which the function *y* is realized. Let element *G* have an input x_i* that is connected directly to the input of the device x_i. On the second input, some function $F_1(x)$ is implemented. Consider the case when an element *G* implements a conjunction and enters into the system of realization of a function f given in disjunctive normal form. In general, such a scheme can be represented in the form of the device shown in Fig. 2.

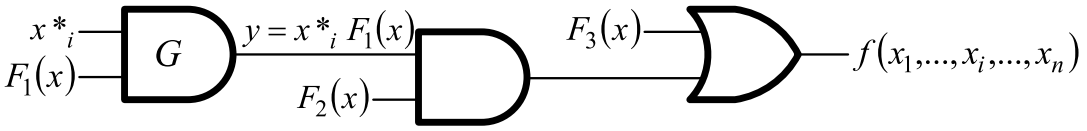

Figure 2. Combinational circuit

The function

$$f(x)=\left(x*_i F_1(x)\right)F_2(x)\vee F_3(x)=yF_2(x)\vee F_3(x), \tag{6}$$

where $F_1(x)$, $F_2(x)$ and $F_3(x)$ are some arbitrary functions of the variables x_1, ..., x_i, ..., x_n, is implemented at the output of the circuit.

The input variable x_i that is fed to the input of the element is indicated with a superscript x_i*. This index means that the failure of the input of the element G corresponds to fixing the variable x_i* to a constant, and the variables x_i received at the inputs of other elements of the circuit are not distorted.

To calculate Boolean differences, we apply the formula

$$\frac{\partial f(x)}{\partial x_i}= \\ =\left[f(x_1,...,x_i,...,x_n)\oplus f(x_1,...,0,...,x_n)\right]\vee\left[f(x_1,...,x_i,...,x_n)\oplus f(x_1,...,1,...,x_n)\right]. \tag{7}$$

In this case, we have (see formulas (6) and (7)): if $x_i*=0$, then $y = 0$ and $f(x_1, ..., 0, ..., x_n) = F_3(x)$; if $x_i^*=1$, then $y=F_1(x)$ and $f(x_1,...,1,...,x_n)=F_1(x)F_2(x)\vee \vee F_3(x)$.

Then

$$\frac{\partial f(x)}{\partial x_i}=\left[f(x)\oplus F_3(x)\right]\vee\left[f(x)\oplus\left(F_1(x)F_2(x)\vee F_3(x)\right)\right]. \tag{8}$$

On the other hand, we have:

$$\frac{\partial f(x)}{\partial x_i}=\left[f(x)\oplus\left(0\cdot F_2(x)\vee F_3(x)\right)\right]\vee\left[f(x)\oplus\left(1\cdot F_2(x)\vee F_3(x)\right)\right]= \\ =\left[f(x)\oplus F_3(x)\right]\vee\left[f(x)\oplus\left(F_2(x)\vee F_3(x)\right)\right]. \tag{9}$$

Let's compare expressions (8) and (9).

Each of the derivatives consists of two functions enclosed in square brackets, which are interconnected by a disjunction sign. Consider the functions enclosed in second square brackets. The relations are

$$F_1(x)F_2(x)\vee F_3(x)\to F_2(x)\vee F_3(x), \tag{10}$$

$$f(x)\oplus\left(F_1(x)F_2(x)\vee F_3(x)\right)\to f(x)\oplus\left(F_2(x)\vee F_3(x)\right). \quad (11)$$

Since in both expressions (8) and (9) the functions enclosed in the first square brackets are identical, it follows from (10) and (11) that

$$\frac{\partial f(x)}{\partial x_i}\to\frac{\partial f(x)}{\partial y}. \quad (12)$$

Thus, the Boolean difference of a variable x_i * contains only those input sets that are included in the Boolean difference of the output of the element *G*.

The theorem is proved.

The Table 3 and 4 shows the Boolean differences for the inputs x_2 and x_3 of the element *G** in the diagram Fig. 1, *a*. From a comparison of the Tables 1 and 3, 4 it follows that relation (12) holds in all cases. For example:

$$\frac{\partial f_1}{\partial y_1(x_2)}=\overline{x}_1x_2x_3\to\frac{\partial f_1}{\partial y_1}=\overline{x}_1x_2,$$

$$\frac{\partial f_2}{\partial y_1(x_3)}=\overline{x}_1x_2\to\frac{\partial f_2}{\partial y_1}=\overline{x}_1\text{, etc.}$$

It can be seen from expression (7) that the Boolean difference combines two checking tests. In the first square brackets, the checking test of the input (or output) of the element for the "stuck-at-0" fault is calculated, and in the second square brackets — for the "stuck-at-1" fault. Therefore, the value of the Boolean difference is determined only

Table 3. The description of the circuit Fig. 1, *a* in case of input x_2 faults

x_1	x_2	x_3	f_1	f_2	f_3	f_4	f_5	$\frac{\partial f_1}{\partial y_1}$	$\frac{\partial f_2}{\partial y_1}$	$\frac{\partial f_3}{\partial y_1}$	$\frac{\partial f_4}{\partial y_1}$	$\frac{\partial f_5}{\partial y_1}$
0	0	0	1	1	1	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0	0	1 (0→1)	0	1 (0→1)	0
0	1	0	0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	1	1	0	1 (1→0)	1 (0→1)	0	1 (1→0)	0
1	0	0	1	1	1	0	0	0	0	0	0	0
1	0	1	1	1	1	0	0	0	0	1 (1→0)	1 (0→1)	1 (0→1)
1	1	0	1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	0	1	1	0	0	1 (0→1)	1 (1→0)	0

Table 4. The description of the circuit Fig. 1, *b* in case of input x_3 faults

x_1	x_2	x_3	f_1	f_2	f_3	f_4	f_5	$\frac{\partial f_1}{\partial y_1}$	$\frac{\partial f_2}{\partial y_1}$	$\frac{\partial f_3}{\partial y_1}$	$\frac{\partial f_4}{\partial y_1}$	$\frac{\partial f_5}{\partial y_1}$
0	0	0	1	1	1	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1 (0→1)	1 (1→0)	1 (1→0)	1 (0→1)	0
0	1	1	1	0	1	1	0	1 (1→0)	1 (0→1)	0	1 (1→0)	0
1	0	0	1	1	1	0	0	0	0	0	0	0
1	0	1	1	1	1	0	0	0	0	0	0	0
1	1	0	1	1	1	1	0	0	0	1 (1→0)	0	1 (0→1)
1	1	1	1	1	0	1	0	0	0	1 (0→1)	1 (1→0)	0

by the values of the functions $f(x_1,...,0,...,x_n)$ and $f(x_1,...,1,...,x_n)$ and does not depend on the structure of the subcircuit, which connects the output of the element *G* with the output of the device, and the structure of the subcircuit that implements the function $F_1(x)$ at the second input of the element *G*, because their verification tests are preserved with equivalent transformations of combinational devices. In this regard, relation (12) is satisfied for any implementation of the function $f(x)$.

Denote by $y_t(x_i)$ the input variable, which is fed to the input of the element G_t. Then the condition under which the input $y_t(x_i)$ failure does not cause a symmetrical error on the set of outputs of the combinational circuit $W = \{f_{j_1}, f_{j_2},..., f_{j_p}\}$ is written as follows:

$$\frac{\partial f_{k_1}}{\partial y_t(x_i)} \cdot \frac{\partial f_{k_2}}{\partial y_t(x_i)} \cdot ... \cdot \frac{\partial f_{k_d}}{\partial y_t(x_i)} \times$$
$$\times \left(\overline{\frac{\partial f_{h_1}}{\partial y_t(x_i)}} \cdot \overline{\frac{\partial f_{h_2}}{\partial y_t(x_i)}} \cdot ... \cdot \overline{\frac{\partial f_{h_{p-d}}}{\partial y_t(x_i)}} \right) Q\left(R_d^{d/2}\left(f_{k_1}, f_{k_2},..., f_{k_d}\right)\right) = 0. \quad (13)$$

Let's compare the expressions (1) and (13). It follows from (12) that $\frac{\partial f_{k_1}}{\partial y_t(x_i)} \to \frac{\partial f_{k_1}}{\partial y_t}$, $\frac{\partial f_{j_2}}{\partial y_t(x_i)} \to \frac{\partial f_{j_2}}{\partial y_t}$, ..., $\frac{\partial f_{k_d}}{\partial y_t(x_i)} \to \frac{\partial f_{k_d}}{\partial y_t}$, $\frac{\partial f_{h_1}}{\partial y_t(x_i)} \to \frac{\partial f_{h_1}}{\partial y_t}$, $\frac{\partial f_{h_2}}{\partial y_t(x_i)} \to \frac{\partial f_{h_2}}{\partial y_t}$, ..., $\frac{\partial f_{h_{p-d}}}{\partial y_t(x_i)} \to \frac{\partial f_{h_{p-d}}}{\partial y_t}$.

Then we have:

$$A\left(y_t\left(x_i\right)\right)=\frac{\partial f_{k_1}}{\partial y_t\left(x_i\right)}\cdot\frac{\partial f_{k_2}}{\partial y_t\left(x_i\right)}\cdot\ldots\cdot\frac{\partial f_{k_d}}{\partial y_t\left(x_i\right)}\to A\left(y_t\right)=\frac{\partial f_{k_1}}{\partial y_t}\cdot\frac{\partial f_{k_2}}{\partial y_t}\cdot\ldots\cdot\frac{\partial f_{k_d}}{\partial y_t},\qquad(14)$$

$$B\left(y_t\left(x_i\right)\right)=\frac{\overline{\partial f_{h_1}}}{\partial y_t\left(x_i\right)}\cdot\frac{\overline{\partial f_{h_2}}}{\partial y_t\left(x_i\right)}\cdot\ldots\cdot\frac{\overline{\partial f_{h_{p-d}}}}{\partial y_t\left(x_i\right)}\to B\left(y_t\right)=\frac{\overline{\partial f_{h_1}}}{\partial y_t}\cdot\frac{\overline{\partial f_{h_2}}}{\partial y_t}\cdot\ldots\cdot\frac{\overline{\partial f_{h_{p-d}}}}{\partial y_t}.\qquad(15)$$

From (14) and (15) it implies that

$$A\left(y_t\left(x_i\right)\right)B\left(y_t\left(x_i\right)\right)\to A\left(y_t\right)B\left(y_t\right).\qquad(16)$$

The validity of statement (1) follows from the fact that in expressions (1) and (13) the third factor C is the same.

For the circuit of Fig. 1, *a* we consider a subset of outputs $\{f_2, f_4\}$ and the fault of input x_2 of the element G^*. Expression (13) has the implies form

$$\frac{\partial f_2}{\partial y_1\left(x_2\right)}\cdot\frac{\partial f_4}{\partial y_1\left(x_2\right)}\cdot\left(\frac{\overline{\partial f_1}}{\partial y_1\left(x_2\right)}\cdot\frac{\overline{\partial f_3}}{\partial y_1\left(x_2\right)}\cdot\frac{\overline{\partial f_5}}{\partial y_1\left(x_2\right)}\right)Q\left(R_d^{d/2}\left(f_2,f_4\right)\right).\qquad(17)$$

We calculate the derivatives (see the Table 3):

$$\frac{\partial f_1}{\partial y_1\left(x_2\right)}=\overline{x}_1x_2x_3,\ \frac{\partial f_2}{\partial y_1\left(x_2\right)}=\overline{x}_1x_3,\ \frac{\partial f_3}{\partial y_1\left(x_2\right)}=x_1x_2,\ \frac{\partial f_4}{\partial y_1\left(x_2\right)}=x_3,$$
$$\frac{\partial f_5}{\partial y_1\left(x_2\right)}=x_1\overline{x}_2x_3.$$

We calculate the following expressions for checking condition (17):

$$A\left(y_t\left(x_2\right)\right)=\frac{\partial f_2}{\partial y_1\left(x_2\right)}\cdot\frac{\partial f_4}{\partial y_1\left(x_2\right)}=(\overline{x}_1x_3)x_3=\overline{x}_1x_3,\qquad(18)$$

$$B\left(y_t\left(x_2\right)\right)=\frac{\overline{\partial f_1}}{\partial y_1\left(x_2\right)}\cdot\frac{\overline{\partial f_3}}{\partial y_1\left(x_2\right)}\cdot\frac{\overline{\partial f_5}}{\partial y_1\left(x_2\right)}=$$
$$=(x_1\vee\overline{x}_2\vee\overline{x}_3)\,(\overline{x}_1\vee\overline{x}_3)\,(\overline{x}_1\vee x_2\vee\overline{x}_3)=\overline{x}_3\vee\overline{x}_1\overline{x}_2.\qquad(19)$$

From a comparison of (18) and (3) it implies that (see (16))

$$\frac{\partial f_2}{\partial y_1(x_2)} \cdot \frac{\partial f_4}{\partial y_1(x_2)} \to \frac{\partial f_2}{\partial y_1} \cdot \frac{\partial f_4}{\partial y_1}.$$

Similarly, a comparison of (19) and (4) implies that

$$\overline{\frac{\partial f_1}{\partial y_1(x_2)}} \cdot \overline{\frac{\partial f_3}{\partial y_1(x_2)}} \cdot \overline{\frac{\partial f_5}{\partial y_1(x_2)}} \to \overline{\frac{\partial f_1}{\partial y_1}} \cdot \overline{\frac{\partial f_3}{\partial y_1}} \cdot \overline{\frac{\partial f_5}{\partial y_1}}.$$

Then

$$A(y_t(x_2))B(y_t(x_2)) = (\overline{x_1}x_3)(\overline{x_3} \vee \overline{x_1}\,\overline{x_2}) =$$
$$= \overline{x_1}\,\overline{x_2}x_3 \to A(y_t)B(y_t) = (\overline{x_1})(\overline{x_1}\,\overline{x_2}x_3) = \overline{x_1}\,\overline{x_2}x_3.$$

From (5) it follows that the fault of the input x_2 of the element G^* admits a symmetrical error. The Theorem 3 allows us to formulate the following statement.

Theorem 4. *When organizing the testing of a combinational circuit according to the UAED (m, k) or d_υ, d_α-UAED (m, k)-code, for detecting all stuck at-faults of the inputs and outputs of logic elements, it is enough to consider only faults of the outputs of logic elements.*

We also note that in combinational circuits, faults may occur in the lines that connect the device input to the inputs of several logic elements. In this case, a multiple malfunction occurs, in which the input signals of several logic elements are fixed into constants. The solution to the problem of detecting faults of this type is possible due to the imposition of certain requirements on the structure of the electrical installation, taking into account the properties of the controlled device [24].

5. The combinational device structure construction

The completely self-checking structure of the combinational circuit is constructed as follows. We find SI-groups of outputs that meet the conditions of the Theorem 2. Each SI-group is controlled using a separate checking based on the *UAED* (m, k) или d_υ, d_α-*UAED* (m, k)-code. The control outputs of all control circuits are combined at the inputs of a self-checking two-rail signal compression circuit to obtain one control output.

The obtaining the required set of SI-groups of outputs, it is advisable to conduct one of the following methods.

The first method is as follows. First, by analyzing all possible subsets of the outputs of the combinational circuit, a complete set of the SI-groups of outputs is found. Then, the minimal subset of the SI-groups is determined, which includes all outputs of the circuit.

In the second method, a set containing all m outputs is considered first. If it does not satisfy the condition of Theorem 2, then all possible subsets with the number of outputs $m-1$, etc., are considered. When the SI-group is found, all the outputs included in it are excluded from further consideration. The process ends when all the outputs of the combinational circuit are included in any SI-group.

The alternative option to search for SI-groups of outputs is a special transformation of the structure of the combinational circuit into a structure whose outputs form a single SI-group. The method for converting circuits into circuits with the SI-groups is similar to that described in [25] for obtaining UI- and UAI-groups.

6. Conclusion

The article revealed and formalized simple conditions under which the selected set of outputs of the combinational circuit forms the SI-group. The search for the SI-groups of outputs on the set of outputs of the circuit, in turn, allows to determine all possible options for splitting into groups of outputs for effective control based on *UAED* (m, k) or d_{υ}, d_{α}-*UAED* (m, k)-codes.

As shown in [18] by the example of searching for UI-groups of outputs, the use of one of the *UAED* (m, k)-codes, the Berger code, makes it possible in practice to organize self-checking discrete devices with redundancy less than when duplicating. In some cases, more than a 50 % reduction in redundancy can be achieved. Expanding the set of outputs to the UAI-group allows to further reduce the redundancy of the self-checking circuit. The same can be concluded for the method of converting circuits into circuits with UAI-outputs, because the conversion will require reservation of a smaller number of internal logic elements than by the method proposed in [18]. As shown in the last source, the complexity of the technical implementation of the original circuit when converted into a device with a controllable structure increases on average by 16 %. The use of UAI-groups in the combinational circuits synthesis can reduce this estimate. The search for the SI-groups of outputs is, in a sense, identical to the search for UAI-groups of outputs, but it is much simpler.

It should be noted that, because the conditions formed are based on the functional principle of describing the operation of a combinational circuit, the results obtained are not oriented only to circuits implemented on logic elements. The field of their application is much wider: the results can be applied to the construction of self-checking combinational circuits on a modern programmable element base.

References

1. *Fujiwara E.* (2006) Code design for dependable systems: Theory and practical applications. New Jersey, John Wiley & Sons Press, 720 p.
2. *Ubar R., Raik J. & Vierhaus H.-T.* (2011) Design and test technology for dependable systems-on-chip (Premier Reference Source). Information Science Reference. Hershey, New York, IGI Global Press, 578 p.

3. *Goessel M., Ocheretny V., Sogomonyan E. & Marienfeld D.* (2008) New methods of concurrent checking. Ed. 1. Dordrecht, Springer Science+Business Media B. V. Press, 184 p.
4. *Nicolaidis M. & Zorian Y.* (1998) On-Line testing for VLSI – A compendium of approaches. *Journal of Electronic Testing: Theory and Application (JETTA)*, vol. 12, iss. 1–2, pp. 7–20. https://doi.org/10.1023/A:1008244815697
5. *Sapozhnikov V. V., Sapozhnikov Vl. V. & Efanov D. V.* (2015) Klassifikaciya oshibok v informacionnyh vektorah sistematicheskih kodov [Errors classification in information vectors of systematic codes]. *Journal of Instrument Engineering*, vol. 58, iss. 5, pp. 333–343. https://doi.org/10.17586/0021-3454-2015-58-5-333-343 (in Russian)
6. *Dmitriev V. V., Efanov D. V., Sapozhnikov V. V. & Sapozhnikov Vl. V.* (2018) Sum codes with efficient detection of twofold errors for organization of concurrent error detection systems of logical devices. *Automation and Remote Control*, vol. 79, iss. 4, pp. 665–678. https://doi.org/10.1134/S0005117918040082
7. *Sapozhnikov V. V., Sapozhnikov Vl. V., Efanov D. V. & Dmitriev V. V.* (2017) New structures of the concurrent error detection systems for logic circuits. *Automation and Remote Control*, vol. 78, iss. 2, pp. 300–313. https://doi.org/10.1134/S0005117917020096
8. *Ghosh S., Basu S. & Touba N. A.* (2005) Synthesis of low power CED circuits based on Parity Codes. *Proceedings of* 23*rd IEEE VLSI Test Symposium (VTS'05)*, pp. 315–320.
9. *Freiman C. V.* (1962) Optimal error detection codes for completely asymmetric binary channels. *Information and Control*, vol. 5, iss. 1, pp. 64–71. https://doi.org/10.1016/S0019–9958 (62)90223–1
10. *Berger J. M.* (1961) A note on error detection codes for asymmetric channels. *Information and Control*, vol. 4, iss. 1, pp. 68–73. https://doi.org/10.1016/S0019–9958 (61)80037–5
11. *Piestrak S. J.* (1995) Design of self-testing checkers for unidirectional error detecting codes. Wrocław, Ofiyna Wydawnicza Politechniki Wrocławskiej Press, 1995, 111 p.
12. *Das D., Touba N. A., Seuring M. & Gossel M.* (2000) Low cost concurrent error detection based on modulo weight-based codes. *Proceedings of the IEEE* 6*th International On-Line Testing Workshop (IOLTW)*. Spain, Palma de Mallorca, July 3–5, pp. 171–176. https://doi.org/10.1109/OLT.2000.856633
13. *Efanov D., Sapozhnikov V. & Sapozhnikov Vl.* (2017) Generalized algorithm of building summation codes for the tasks of technical diagnostics of discrete systems. *Proceedings of* 15*th IEEE East-West Design & Test Symposium (EWDTS'2017)*. Novi Sad, Serbia, September 29 – October 02, pp. 365–371. https://doi.org/10.1109/EWDTS.2017.8110126
14. *Sogomonyan E. S. & Slabakov E. V.* (1989) Samoproveryaemye ustrojstva i vychislitel'nye sistemy [Self-checking devices and fault-tolerant systems]. Moscow, Radio & Communication Publ., 208 p. (in Russian)
15. *Goessel M. & Sogomonyan E. S.* (1992) Formation of self-testing and self-checking combinational circuits with weakly independent outputs. *Automation and Remote Control*, vol. 53, iss. 8, pp. 1264–1272.
16. *Sogomonyan E. S. & Gossel M.* (1993) Design of self-testing and on-line faul detection combinational circuits with weakly independent outputs. *Journal of Electronic Testing: Theory and Applications*, vol. 4, iss. 4, pp. 267–281. https://doi.org/10.1007/BF00971975
17. *Busaba F. Y. & Lala P. K.* (1994) Self-checking combinational circuit design for single and unidirectional multibit errors. *Journal of Electronic Testing: Theory and Applications*, vol. 5, iss. 1, pp. 19–28. https://doi.org/10.1007/BF00971960
18. *Morosow A., Sapozhnikov V. V., Sapozhnikov Vl. V. & Gossel M.* (1998) Self-checking combinational circuits with unidirectionally independent outputs. *VLSI Design*, vol. 5, iss. 4, pp. 333–345. https://doi.org/10.1155/1998/20389

19. *Efanov D. V., Sapozhnikov V. V. & Sapozhnikov Vl. V.* (2018) Synthesis of self-checking combinational devices based on allocating special groups of outputs. *Automation and Remote Control*, vol. 79, iss. 9, pp. 1607–1618. https://doi.org/10.1134/S0005117918090060
20. *Sapozhnikov V. V., Sapozhnikov Vl. V. & Efanov D. V.* (2018) Kody Hemminga v sistemah funkcional'nogo kontrolya logicheskih ustrojstv [Hamming Codes in concurrent error detection systems of logic devices]. Saint Petersburg, Nauka Publ., 2018, 151 p. (in Russian)
21. *Das D. & Touba N. A.* (1999) Synthesis of circuits with low-cost concurrent error detection based on bose-lin codes. *Journal of Electronic Testing: Theory and Applications*, 1999, vol. 15, iss. 1–2, pp. 145–155. https://doi.org/10.1023/A:1008344603814
22. *Efanov D. V., Sapozhnikov V. V. & Sapozhnikov Vl. V.* (2015) Application of modular summation codes to concurrent error detection systems for combinational boolean circuits. *Automation and Remote Control*, vol. 76, iss. 10, pp. 1834–1848. https://doi.org/10.1134/S0005117915100112
23. *Efanov D. V., Sapozhnikov V. V. & Sapozhnikov Vl. V.* (2017) Conditions for detecting a logical element fault in a combination device under concurrent checking based on Berger`s Code. *Automation and Remote Control*, vol. 78, iss. 5, pp. 892–902. https://doi.org/10.1134/S0005117917040113
24. *Prokofjev A. A., Sapozhnikov V. V. & Sapozhnikov Vl. V.* (1984) Logicheskij metod kontrolya elektricheskogo montazha [Logical testing method for electrical arrangement]. *Electronic Modeling*, vol. 6, iss. 4, pp. 55–59. (in Russian)
25. *Sapozhnikov V., Sapozhnikov Vl. & Efanov D.* (2017) Search Algorithm for fully tested elements in combinational circuits, controlled on the basis of Berger Codes. *Proceedings of 15th IEEE East-West Design & Test Symposium (EWDTS'2017)*. Novi Sad, Serbia, September 29 – October 02, pp. 99–108. https://doi.org/10.1109/EWDTS.2017.8110085

The paper is submitted for publication by Raimund Ubar, a member of the editorial board.
Received: May 19, 2020, accepted: June 01,2020

В. В. Сапожников, д-р техн. наук
Вл. В. Сапожников, д-р техн. наук

Кафедра «Автоматика и телемеханика на железных дорогах»
Петербургский государственный университет путей сообщения
Императора Александра I, Санкт-Петербург

Д. В. Ефанов, д-р техн. наук

ООО «ВЕГА Групп», Санкт-Петербург
Высшая школа транспорта Института машиностроения, материалов и транспорта
Санкт-Петербургский политехнический университет Петра Великого, Санкт-Петербург
Кафедра «Автоматика, телемеханика и связь на железнодорожном транспорте»
Российский университет транспорта, Москва

ОСОБЕННОСТИ ПОСТРОЕНИЯ СИСТЕМ ФУНКЦИОНАЛЬНОГО КОНТРОЛЯ КОМБИНАЦИОННЫХ ЛОГИЧЕСКИХ СХЕМ НА ОСНОВЕ ПОИСКА ГРУПП СИММЕТРИЧНО-НЕЗАВИСИМЫХ ВЫХОДОВ

В статье установлено, что при применении классических кодов с суммированием (кодов Бергера) и ряда их модификаций при организации контроля комбинационных схем можно использовать их особенности обнаружения как монотонных, так и части немонотонных ошибок в информационных векторах. Показано, что возможен поиск групп выходов комбинационных схем, на которых могут возникать только симметричные ошибки вследствие одиночных неисправностей элементов внутренней структуры схем. Такие группы выходов обозначены как группы симметрично-независимых выходов. Определены условия принадлежности группы выходов комбинационной схемы к группам симметрично-независимых выходов. Показано, что каждая симметрично-независимая группа выходов может контролироваться при помощи отдельной подсистемы контроля на основе кода с обнаружением любых несимметричных ошибок (в частности, и любых несимметричных ошибок до определенных кратностей). Представлены пути поиска групп симметрично-независимых выходов при организации контроля комбинационных схем.

Комбинационная схема, самопроверяемая структура, монотонная ошибка, симметричная ошибка, асимметричная ошибка, код с обнаружением монотонных и асимметричных ошибок, группы симметрично-независимых выходов

DOI: 10.20295/2412-9186-2020-6-4-532-549

САПОЖНИКОВ Валерий Владимирович — доктор технических наук, профессор кафедры «Автоматика и телемеханика на железных дорогах» Петербургского государственного университета путей сообщения Императора Александра I

e-mail: port.at.pgups1@gmail.com

САПОЖНИКОВ Владимир Владимирович — доктор технических наук, профессор кафедры «Автоматика и телемеханика на железных дорогах» Петербургского государственного университета путей сообщения Императора Александра I

e-mail: sapozhnikov-at@yandex.ru

ЕФАНОВ Дмитрий Викторович — доктор технических наук, доцент, первый заместитель генерального директора — главный инженер ООО «ВЕГА Групп», профессор Высшей школы транспорта Института машиностроения, материалов и транспорта Санкт-Петербургского политехнического университета Петра Великого, профессор кафедры «Автоматика, телемеханика и связь на железнодорожном транспорте» Российского университета транспорта

e-mail: TrES-4b@yandex.ru